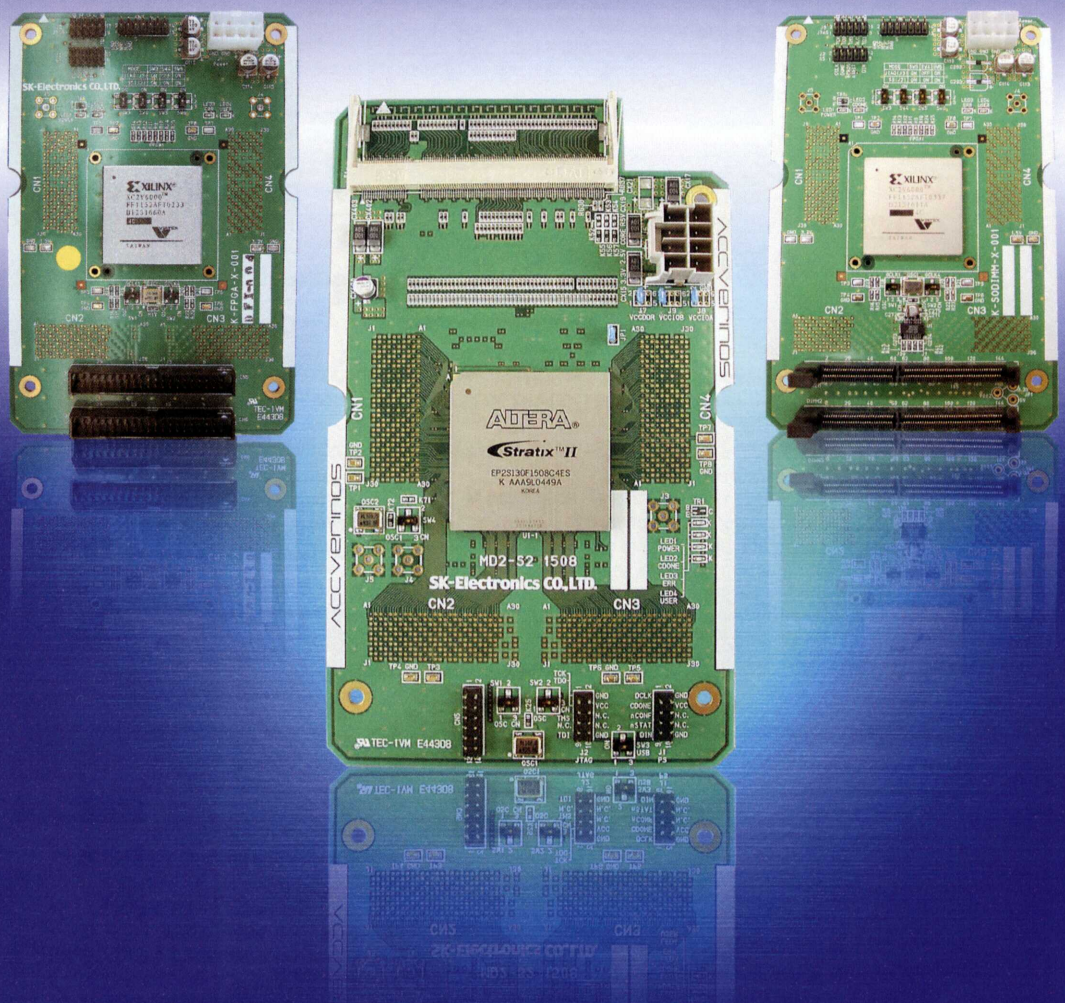
Product Family Catalog

Jan. 2006

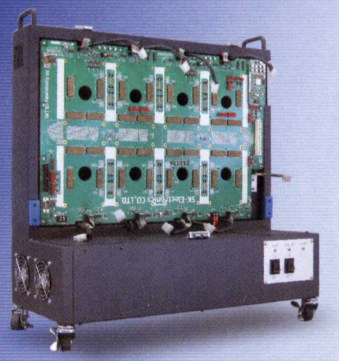
ACCVerinos



SK-Electronics CO.,LTD.

Base Systems

The Base System applies any kind of Large Gate Count verification environment, and assures its high-speed data transfer.



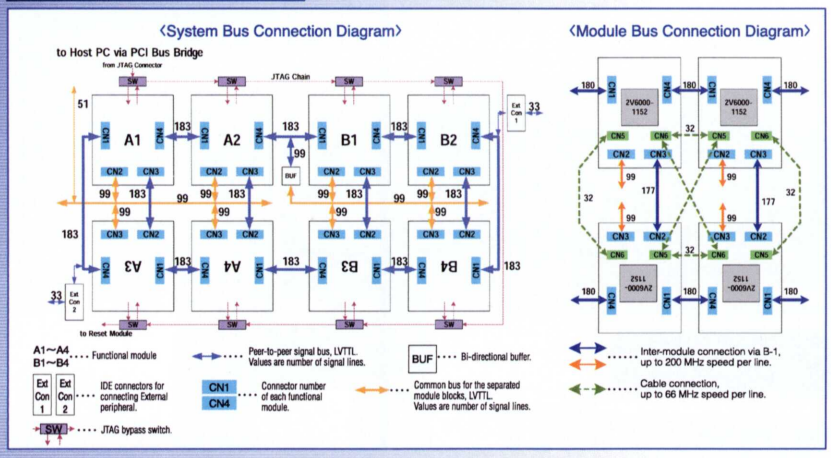
620 mm (W) X 670 mm (H) X 188 mm (D)
(Excluding handles and casters)

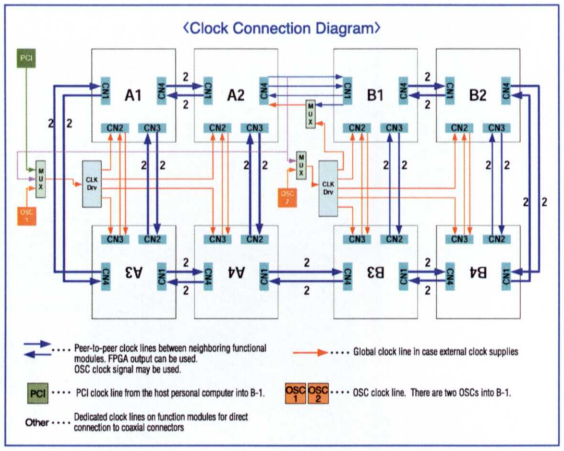
B-1 Base System: Large Gate Count Verification System

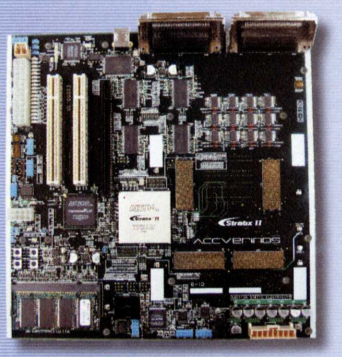
Useable with up to eight functional modules mounted. Total 4M - 10M ASIC gate count circuit can be contained. Assures up to 200 MHz speed data transfer, each other.

- Interfaces: PCI, signal monitoring connectors, extension connectors, Switches, and LEDs
- PCI bridge can be applied: PCI-bus of personal computer can be connected to B-1 Base System.
- Dedicated signal lines (Clock, JTAG, Reset):
- Clock lines (there are two clock signal lines.): Peer-to-peer clock lines between neighboring functional modules
  Individual global clock signal lines for the separated functional module block (see the following figure.)
- JTAG chains, reset and control lines
- Configuration scheme: All functional modules can be configured by using JTAG-chain on B-1 Base System.
  Stand-alone configuration also available.
- Each functional module connects to its own power source
- B-1 Base System contains PLD reset control module and DC power supply module for each functional module.
- Chassis: choose from metal type or acrylic type.

Functional Block Connection Diagrams







244 mm X 244 mm

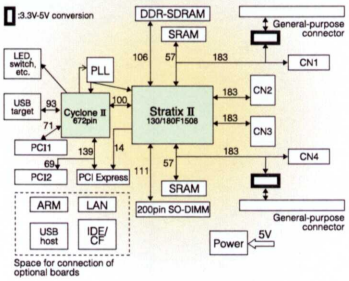
New release B-10 Base System: Compact Size Verification System

ALTERA. Stratix II

Compact prototyping verification system with Altera Stratix II, DDR memory, and flexible connectivity.

- DDR memory module: 200-pin SO-DIMM PC3200 (200/400 MHz), 512 MB
- On-board memory: PC3200 (200/400 MHz) DDR memory, 512 MB
  fast SRAM, 16 M-bits
- FPGA: Altera Stratix II EP2S130F1508 (EP2S180F1508 may available)
- Interface: USB 2.0 and PCI
- Accverinos series functional module can be mounted (Assured 200 MHz data transfer speed between B-10 and the functional module).
- Maximum 2M ASIC gate count circuit
  (when using EP2S180 and M-10 functional module)
- Flexible connectivity by using PCI board or custom interface board
- Chain connectivity with multiple B-10 Base Systems
- Total 780 user I/O (excluding memory interfaces)
- Gated-clock can be realized on B-10 Base System.
- Micro ATX chassis (easy to use)
- Sample FPGA circuit core-IP and PC base software
- Sample software (Windows driver and application software) supplied as source code.

Functional Block Diagram



Release scheduled for March 2006

NOW PRINTING

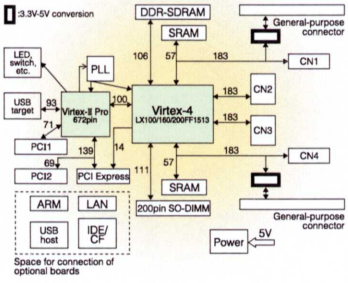
244 mm X 244 mm

B-20 Base System: Compact Size Verification System

Compact prototyping verification system with Xilinx Virtex-4, DDR memory, and flexible connectivity.

- DDR memory module: 200-pin SO-DIMM PC2700 (166/333 MHz),
  512 MB, fast SRAM, 16 M-bits
- On-board memory: PC2700 (166/333 MHz) DDR memory, 512 MB
- FPGA: Xilinx Virtex-4 XCE4VLX100/160/200-FF1513
- Interface: USB 2.0 and PCI
- Accverinos series functional module can be mounted (Data transfer speed between B-20 and the functional module is assured up to 200 MHz).
- Maximum 2M ASIC gate count circuit (when using XCE4VLX200 and M-20 functional module)
- Flexible connectivity by using PCI board or custom interface board
- Chain connectivity with multiple B-20 Base Systems
- Gated-clock can be realized on B-20 Base System.
- Micro ATX Chassis (easy to use)
- Sample FPGA circuit core-IP (memory controller) and PC base software
- Sample software (Windows driver and application software) supplied as source code.

Functional Block Diagram



Functional modules

A lineup of highly functional, high-precision modules Precisely meeting differing needs and environments

105 mm (W) × 155 mm (H) × 34 mm (D)

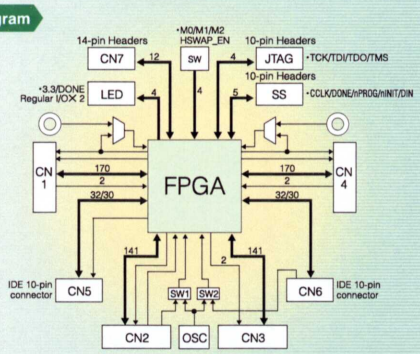
M-1: FPGA Functional Module

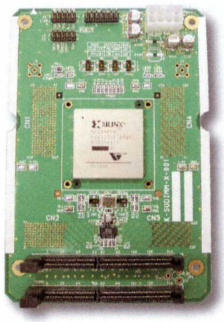
Virtex-II FPGA module

- Accverinos series functional module
- Assuring 100 MHz speed data transfer (160 signal lines in parallel) between neighboring functional modules on Accverinos B-1.※1
- FPGA: Xilinx XC2V6000-FF1152 (XC2V8000-FF1152 also available.)
- Total 698 user I/Os
- Contains two IDE connectors, (each IDE has 32 user I/Os and a dedicated clock.)
- FPGA function DCI (digitally controlled impedance) may be available.
- Design Gateway configuration supports: FlashLink
- Sample FPGA circuit core-IP (Verilog: PCI and inter-connect test circuit between functional modules) and PC base software (Windows driver and application software) source code may be applied.

※1:Circuit testing conducted by SK-Electronics (source attached to product as sample)

Functional Block Diagram





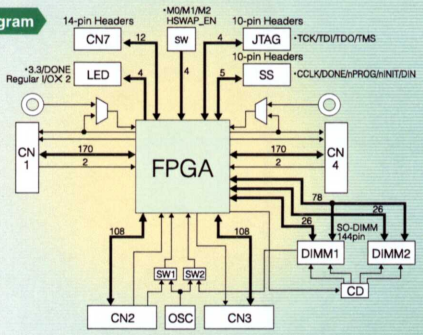
105 mm (W) × 155 mm (H) × 46 mm (D)

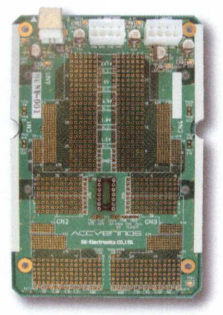
M-2: FPGA Functional Module

Virtex-II FPGA module with SDRAM module, 133MHz

- Memory module: 144-pin SO-DIMM 133 MHz, 256MB (up to 512 MB may be available.)
- FPGA: Xilinx XC2V6000-FF1152 (XC2V8000-FF1152 also available.)
- Up to 8 of M-2 modules can be mounted on B-1.
- Total 556 user I/Os
- FPGA function DCI (digitally controlled impedance) may be available.
- Design Gateway configuration supports: FlashLink
- Sample FPGA circuit core-IP (memory controller and PCI) and PC base software (Windows driver and application software) source code may be applied.

Functional Block Diagram





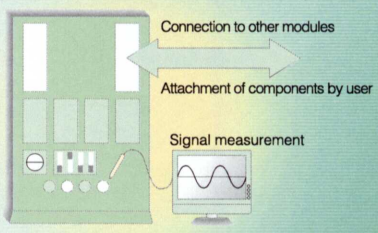
105 mm (W) × 155 mm (H) × 34 mm (D)

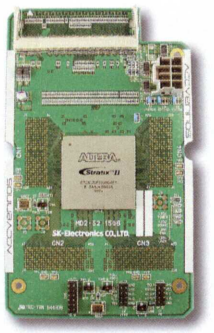
M-3: General Purpose Module

Original user circuits can be easily implemented.

- Off-the-shelf devices and a variety of connectors can be mounted.
- Flexible connectivity to other functional modules or external peripheral
- Easy to Monitor Input/Output signals

Example of Use





105 mm (W) × 175 mm (H) × 34 mm (D)

New release M-10: FPGA Functional Module

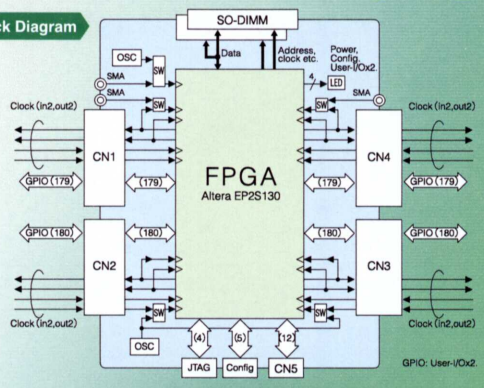
ALTERA. Stratix II

Altera Stratix II FPGA module with SO-DIMM DDR 200/400 MHz module

- Memory module: two 200-pin SO-DIMM DDR 200/400 MHz, mounted on the surface and the back side. Off-the-shelf PC3200 DDR memory module (for laptop PC) can be used.※1
- FPGA: Altera Stratix II FPGA (EP2S130FF1508)※2
- Up to 8 functional modules can be mounted on B-1 Base System.
- Total 730 user I/Os (excluding DDR memory module interface).
- Altera configuration cable supports; Byte Blaster II, Byte Blaster MV, USB-Blaster and Master Blaster serial/USB Communication Cable Altera configuration cable
- Design Gateway configuration supports: FlashLink and JtagLink

※1:confirmed by using Altera MegaCore DDR & DDR2 SDRAM Controller. PC3200 is limited to use on only one side (either surface or back side).
※2:EP2S180-F1508 may be available.

Functional Block Diagram



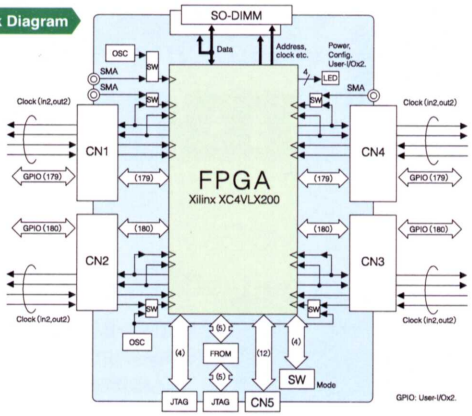
105 mm (W) × 175 mm (H) × 34 mm (D)

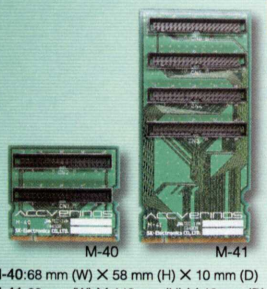
New release M-20: FPGA Functional Module

Xilinx Virtex-4 FPGA module with SO-DIMM DDR 166/333 MHz module

- Memory module: two 200-pin SO-DIMM DDR 166/333 MHz, mounted on surface and back side
  Off-the-shelf PC2700 DDR memory module (for laptop PC) can be used.
- FPGA: Xilinx Virtex-4 FPGA (XCE4VLX100/160/200-FF1513)
- Supports Design Gateway configuration tools: FlashLink and JtagLink

Functional Block Diagram





M-40 M-41

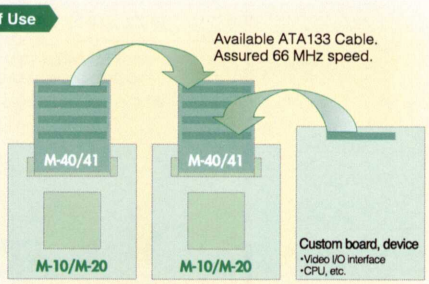
M-40:68 mm (W) × 58 mm (H) × 10 mm (D)
M-41:68 mm (W) × 140 mm (H) × 10 mm (D)

New release M-40/41: SO-DIMM Extension Module (IDE type connection)

Connector module for connecting to external peripherals, equipment

- Use by attaching SO-DIMM memory sockets on M-10/M-20 FPGA functional module
- Total of six IDEs with M-40 and M-41 combined
- Assured 66 MHz speed data transfer
- M-40 for surface side, M-41 for back side of M-10/M-20

Example of Use



Symbols Used in Functional Block Diagrams

Clock (Values are number of clocks) | Other bus signal line (179) (Values are number of lines) | SW DIP switch | OSC Crystal oscillator | SMA connector mounting area | Selection area using ΩW resistance

Service and Support

ACCVERINOS offers the real-time verification process from the proposal of system solutions to the development of full custom.

Hardware Support

- Standard Base Systems
- Custom Base Systems
- Standard Function Modules
- Custom Function Modules
- IP Cores / FPGA Mapping / ASIC Mapping
- Circuit Design / Verification Services

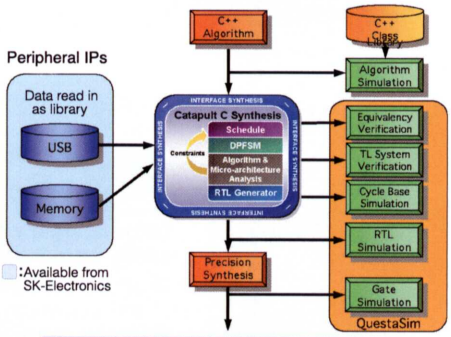
Software Support

- Provision of Sample Circuit Sources
- Circuit Drawing Disclosure
- Synplicity Development Tools
  •Synplify Pro •Identify •Certify
- Altera Development Tools
  •Quartus II
- Xilinx Development Tools
  •ISE •ChipScope

ACCVERINOS is suitable for these high-speed, high-volume data processing applications.

- System LSI
- Image/video processing
- RF-IC
  (In partnership with Telemidic Co., Ltd. http://www.telemidic.com)

Libraries for Catapult C Synthesis Provided



ACCVERINOS Product Family

- A high-speed verification solution made available by Mentor Graphics Japan and SK-Electronics that can be put to use immediately by system-level developers.
- Environments now planned to be made available to allow data from Catapult C Synthesis to be seamlessly implemented to the Accverinos family of verification boards offering over 200MHz.
- Libraries necessary for peripheral circuitry will gradually be made available by SK-Electronics together with its operationally proven hardware.

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All information contained herein is current as of January 2006.

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